

# A Non-uniform DPLL Architecture for Optimized Performance

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This paper presents the design, analysis, simulation and implementation of the architecture of a new non-uniform type digital phase-locked loop (DPLL). The proposed loop uses a composite phase detector (CPD), which consists of a sample-and-hold unit and an arctan block. The CPD improves the system linearity and results in a wider lock range. In addition, the loop has an adaptive controller block, which can be used to minimize the overall system sensitivity to variations in the power of the input signal. Furthermore, the controller has a tuning mechanism that gives the designer the flexibility to customize the loop parameters to suit a particular application. These performance parameters include lock range, acquisition time, phase noise or jitter, and signal to noise ratio enhancement. The simulation results show that the proposed loop provides flexibility to optimize the major conflicting system parameters. A prototype of the proposed system was implemented using an FPGA and the practical results concur with those obtained by simulation using MATLAB/Simulink.

**Keywords:** Acquisition time, composite phase detector, digital phase-locked loop, jitter, lock range, noise.

## 1. Introduction

The phase-locked loop (PLL) is a crucial building block in many electronic systems where phase tracking and synchronization, clock recovery and re-generation and/or clock distribution are required. Basically, a PLL is a feedback control system that generates an output signal whose phase is related to the phase of the input “or reference” signal. For a first-order loop, the phase difference between the two signals in the locked state is a non-zero constant, whilst for a second- or higher-order loop, the phase difference, also known as the steady-state phase error, is zero<sup>(1)–(3)</sup>. The applications of PLLs have grown to span a wide spectrum of systems including various communications, control, and signal processing systems<sup>(4)–(5)</sup>. Frequency synthesizers in RF communication systems are typical applications in which PLLs are used for clock extraction and generation<sup>(6)</sup>.

Early PLLs were analogue devices and consequently suffered some drawbacks such as component tolerance, sensitivity to DC drift, and difficulties in creating higher order loops. Many of these problems were alleviated by the introduction of digital PLLs (DPLLs). Because one of the major processes in a DPLL is sampling of analogue signals, DPLLs are usually classified as uniform and non-uniform according to the nature of the applied sampling process. A uniform DPLL type uses a fixed clock sampling process, which limits the speed performance of the loop while non-uniform DPLLs achieve better speed performance with less circuit complexity than their uniform counterpart<sup>(7)–(8)</sup>.

The zero crossing DPLL (ZC-DPLL), depicted in Fig. 1, is an architecture that uses non-uniform sampling, and is widely used due to its modeling and implementation simplicity. However, the ZC-DPLL is sensitive to variations in the power of the input signal, which can significantly degrade its performance. In addition, the ZC-DPLL inherent non-linearity imposes limitation on its lock range which may have hindered its success<sup>(4),(9)–(13)</sup>.

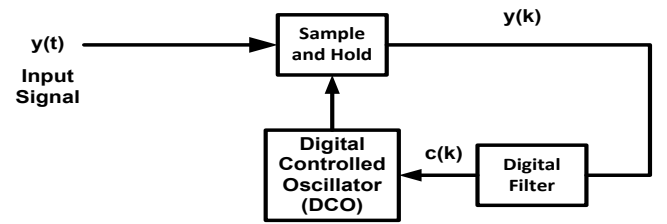


Fig.1. Block diagram of the zero-crossing digital phase-locked loop.

This paper presents an enhanced ZC-DPLL system level architecture that overcomes the aforementioned limitations. This is achieved by modifying the phase detector which has a major effect on the overall performance of the ZC-DPLL. Various designs of the phase detector have been reported in the literature with the aim of resolving issues related to the system performance such as the lock range and system linearity<sup>(1),(2),(4)</sup>. In this work a composite phase detector (CPD) consisting of a combination of a sample-and-hold and an arctan blocks is used. This new detector offers the advantage of improved linearity and hence wider lock range capability. In addition, an adaptive controller block was added to the proposed loop. This allows optimization of the lock range, acquisition time, noise immunity, and sensitivity to variations in the input signal power, with due account of a given application requirements. With these modifications, the proposed composite phase detector DPLL system, henceforth referred to as CPD-DPLL, overcomes the two main limitations of the conventional ZC-DPLL, namely linearity and sensitivity to the variations in the input signal power<sup>(14)–(16)</sup>. The proposed system level architecture CPD-DPLL, which is shown in Fig. 2, consists of a CPD, digital filter, digital controlled oscillator (DCO), and the adaptive controller.

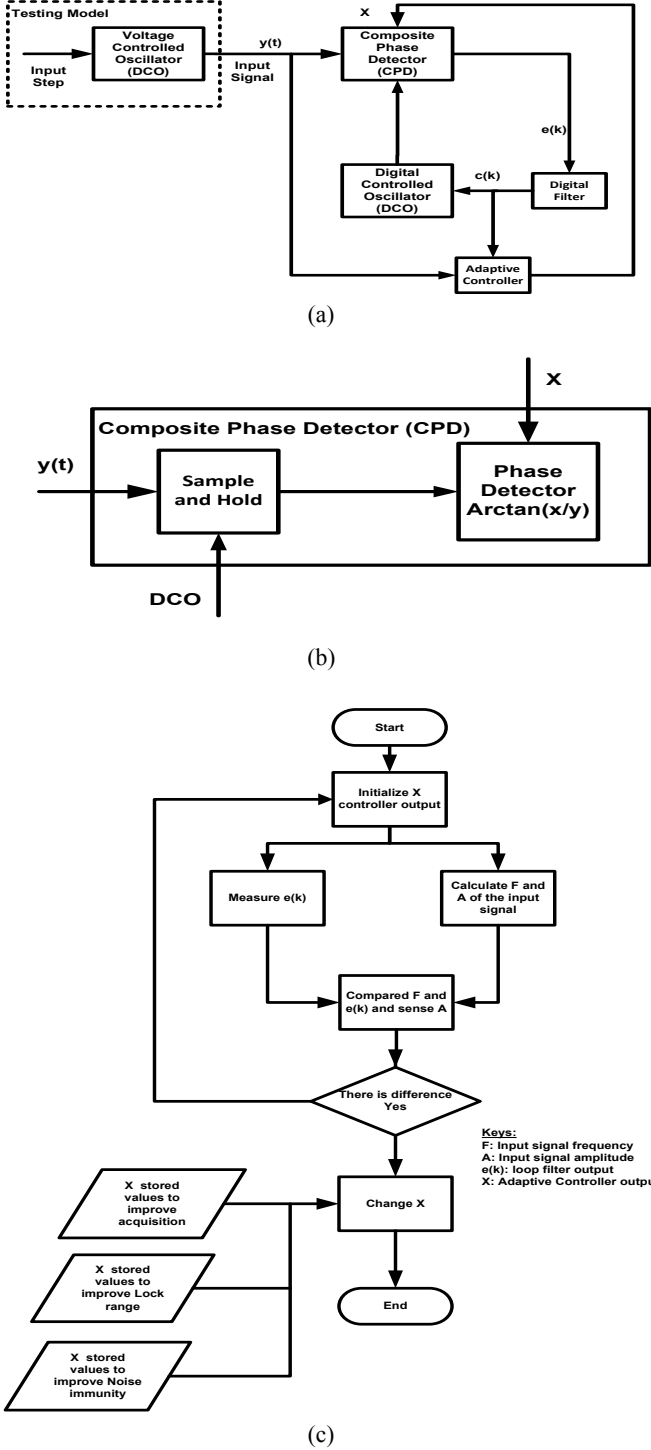


Fig. 2. Block diagram of (a) CPD-DPLL and (b) CPD phase detector (c) adaptive controller functional flowchart.

The CPD, Fig. 2 (b), uses the adaptive controller output  $X$  so as to optimize particular loop performance parameters to best match the requirements of a given application. The adaptive controller algorithm is illustrated in the flowchart of Fig. 2 (c). The algorithm simply starts with initializing the adaptive controller output  $X$ . Then an evaluation and sensing of both frequency and amplitude of the incoming signal with the aim of re-mapping  $X$  values in order to enhance the locking range, linearity, and acquisition speed as will be detailed in the following sections.

The remainder of this paper is organized as follows: Section 2

presents the mathematical analysis of the first-order CPD-DPLL system. The system noise analysis is presented in section 3. The simulation results are discussed in section 4, whilst the hardware implementation of the system using a field programmable gate array (FPGA) is described in section 5. Finally, the conclusions of the work are presented section 6.

## 2. CPD-DPLL System Analysis

In the analysis of the CPD-DPLL system of Fig. 2, it is assumed that the input to the loop is a continuous time dependent sinusoidal signal as in (1)

$$y(t) = A \sin[\omega_o t + \theta(t)] \quad (1)$$

where  $A$  is the amplitude of the signal,  $\omega_o$  (rad/s) is the free running frequency of the DCO, and  $\theta(t)$  is the information bearing phase in radians. Assuming a frequency step at the input, the phase of the phase process will be

$$\theta(t) = (\omega - \omega_o)t + \theta_o \quad (2)$$

where  $\omega$  (rad/s) is the angular frequency of the input signal and  $\theta_o$  (rad) is a constant. The discretized signal generated by the sampler is

$$y(k) = A \sin[\omega_o t(k) + \theta(k)] \quad (3)$$

where  $t(k)$  is the total time elapsed up to the  $k^{\text{th}}$  sampling instant. The sampling interval of the DCO between the sampling instants  $t(k+1)$  and  $t(k)$  is given by

$$T(k) = T_o - c(k-1) \quad (4)$$

where  $T_o = 2\pi/\omega_o$  (s) is the free running period of the DCO, while  $c(k-1)$  is the output of the digital filter at the previous sampling instant. The total time up to the  $k^{\text{th}}$  sampling instant can be defined as

$$t(k) = \sum_{i=1}^k T(i) = kT_o - \sum_{i=0}^{k-1} c(i) \quad (5)$$

Substituting (5) in (3)

$$y(k) = A \sin\left[\theta(k) - \omega_o \sum_{i=0}^{k-1} c(i)\right] \quad (6)$$

Therefore, the phase error between the input signal and the output of the DCO is given by

$$\phi(k) = \theta(k) - \omega_o \sum_{i=0}^{k-1} c(i) \quad (7)$$

Consequently, (6) can be re-written as

$$y(k) = A \sin[\phi(k)] \quad (8)$$

The digitized input signal  $y(k)$  and adaptive controller output  $X$  are applied to the arctan phase detector producing the error signal  $e(k)$ , which is also known as the characteristic function  $h(\phi)$  of the phase detector

$$e(k) = h(\phi) = f\left[\tan^{-1}\left(\frac{A \sin[\phi(k)]}{X}\right)\right] \quad (9)$$

where  $f(\gamma) = -\pi + [(\gamma + \pi) \bmod 2\pi]$

The error signal  $e(k)$  is the input to the digital filter whose transfer function is  $D(k)$  and its output is the signal  $c(k)$  which drives the DCO. For a first-order CPD-DPLL, the DCO is simply a gain block with a gain  $G_1$ . Therefore, the system difference equation can be derived from (5), (8) and (9). This equation can be defined as

$$\phi(k+1) = \phi(k) - K'_1 h[\phi(k)] + \Lambda_o \quad (10)$$

$$\phi(k+1) = \phi(k) - K'_1 \left[ \tan^{-1} \left( \frac{A \sin[\phi(k)]}{X} \right) \right] + \Lambda_o \quad (11)$$

where  $K'_1 = \omega G_1$  and  $\Lambda_o = 2\pi(\omega - \omega_o)/\omega_o$

Defining  $K_1 = \omega_o G_1$  results in  $K'_1 = K_1/W$ , where  $W = \omega_o/\omega$ . Due to the nonlinearity and following similar analysis as in <sup>(17)</sup>, the lock range of the first-order loop can be determined by numerically solving the inequality

$$2|1-W| < K_1 < 2W \frac{A^2 \sin^2(\alpha) + X^2}{AX \cos(\alpha)} \quad (12)$$

where  $\alpha = \arcsin(\beta)$ ,  $\beta = \frac{X}{A} \tan(\eta)$  and  $\eta = \frac{\Lambda_o}{K'_1}$

The steady-state phase error  $\phi_{ss}$  is <sup>(17)</sup>

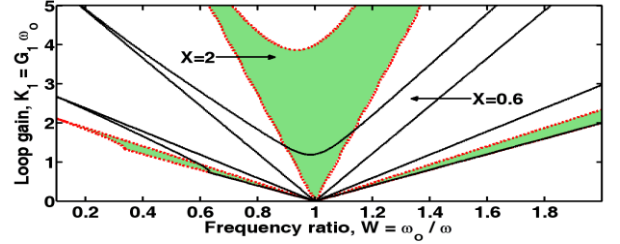
$$\phi_{ss} = \alpha + j\pi, \quad j \in \{1, 0, -1\} \quad (13)$$

Fig. 3 (a) and (b), plotted using (12), depict changes in the lock range of the first-order CPD-DPLL as a function of both input signal amplitude (A) and the input controller (X) produced by the adaptive controller. Fig. 3 (a) shows the behavior of the CPD-DPLL for various values of X at A=1 V.

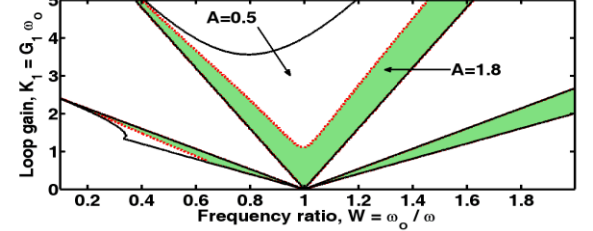
Fig. 3 (b) illustrates changes in the lock range for various input signal amplitudes when X=1 V. Fig. 3 (c) shows the lock range of the conventional non-uniform ZC-DPLL and allows comparison with that of the CPD-DPLL <sup>(13)</sup>. The lock range in Fig. 3 (c) is fixed; the system designer does not have the flexibility the adaptive controller offers in the proposed CPD-DPLL system. This is plotted using the inequality <sup>(13)</sup>

$$2|1-W| < K_1 < \sqrt{(4 + (2\pi)^2)W^2 - 2(2\pi)^2W} + (2\pi)^2$$

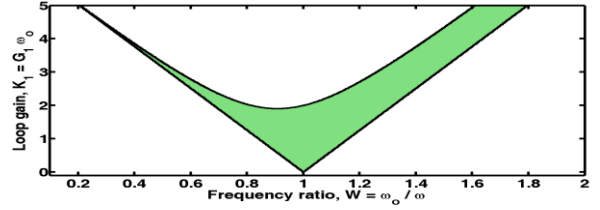
From the plots in Fig. 3 (a) and (b), and for an operating condition of  $K_1=1$  and  $W=1$ , the lock range can be customized to match a given set of application requirements. For example, for a  $0.6 \text{ V} \leq X \leq 2 \text{ V}$ , the loop can operate under input signal amplitude in the range of  $0 \text{ V} \leq A \leq 1.8 \text{ V}$ . The ability to control the major loop parameters through the appropriate choice of the adaptive controller output X, while A is within the above range, can solve the conflicting requirement for a wider lock range and faster acquisition speed. This also affects the noise performance of the system which will be addressed in Section 3. Further, if the adaptive controller output X is used to follow the amplitude A in the above range then a fairly fast acquisition system can be designed as will be explained Section 4. The following subsections present analysis of the various performance parameters of the proposed loop.



(a) Lock range of CPD-DPLL with A=1 and changing X



(b) Lock range of CPD-DPLL with X=1 and changing A



(c) Lock range of conventional ZC-DPLL

Fig. 3. Lock range of the first-order (a) CPD-DPLL with A=1 and changing X (b) CPD-DPLL with X=1 and changing A and (c) conventional ZC-DPLL.  $K_1 = \omega_o G_1$  and  $W = \omega_o/\omega$ .

**2.1 System Lock Range** To allow control and hence optimization of the lock range, the adaptive controller output X is expressed as

$$X = f_1 \left[ \frac{A \sin[\alpha(k) + \theta_o]}{\tan\left(\frac{c(k)}{G_1}\right)} \right] = f_1 \left[ \frac{y(t)}{\tan\left(\frac{c(k)}{G_1}\right)} \right] \quad (14)$$

where  $f_1(\gamma) = (\gamma + \pi) \bmod 2\pi$ ,  $y(t)$  is the input signal while, A is the amplitude,  $\omega$ (rad/s) is frequency and  $\theta_o$  is the initial phase in radians, of the input signal. From (14) it is evident that the adaptive controller output X is a function of both the amplitude and frequency of the input signal. Therefore, the performance in terms of acquisition and lock range can be controlled through the CPD phase detector using the value of X.

From (14) it is also evident that the adaptive controller output X is proportional to the input signal amplitude A via a nonlinear factor which is controlled by the incoming signal frequency, the output of the loop filter, and the initial phase. To reduce the loop sensitivity to the incoming signal amplitude, the adaptive controller output X value should be at least equal to A or higher. This ensures that any degradation in the performance of the loop is negligible as long as the amplitude of the input signal is less than the value of adaptive controller output X.

Therefore, to obtain maximum linearity, the characteristic equation (11) can be modified to

$$\phi(k+1) = \phi(k) - K'_1 \phi(k) + \Lambda_o \quad (15)$$

From (15), proper design of the adaptive controller can ensure

linear characteristic equation. Using (12) and (14) the lock range can be re-expressed as

$$2|1-W| < K_1 < 2W \frac{A^2 \sin^2(\alpha) + \left[ \frac{y(t)}{\tan\left(\frac{c(k)}{G_1}\right)} \right]^2}{A \left[ \frac{y(t)}{\tan\left(\frac{c(k)}{G_1}\right)} \right] \cos(\alpha)} \dots\dots\dots (16)$$

From (16), it is shown that with a proper re-scaling values of both amplitude and frequency of the incoming signal in addition to the filter output  $c(k)$  the lock range can be set to a desired value.

**2.2 System Acquisition** The analysis in this subsection shows the effect of the controller output  $X$  on the convergence speed of the CPD-DPLL system. Using the fixed-point analysis developed in <sup>(10),(13)</sup> the steady-state phase error can be written as

$$\phi_{ss} = \begin{cases} \alpha & \beta \sin(\eta) \geq 0 \\ f[\alpha + \pi] & \text{otherwise.} \end{cases} \dots\dots\dots (17)$$

where  $\alpha = \arcsin(\beta)$ ,  $\beta = \frac{X}{A} * \tan(\eta)$  and  $\eta = \frac{\Lambda_o}{K'_1}$

The characteristic function of the phase detector and its first derivative are continuous and hence differentiable in the principal interval  $(-\pi, \pi)$  therefore, fixed-point analysis is applicable to the CPD-DPLL. Following fixed-point analysis developed in <sup>(10),(13),(16)</sup> for the sinusoidal digital phase-locked loop, the Lipschitz constant is given by

$$L = \max \left| \frac{g(\phi) - g(\phi_{ss})}{\phi - \phi_{ss}} \right| \dots\dots\dots (18)$$

where  $g(\phi)$  can be expressed as

$$g(\phi) = \phi - K'_1 \left[ \tan^{-1} \left( \frac{A \sin[\phi(k)]}{X} \right) \right] + \Lambda_o \dots\dots\dots (19)$$

The asymptotic estimate (upper bound) to the number of steps required for convergence of the phase error  $\phi(k)$  to within a small radius  $\epsilon$  of the fixed point  $\phi_{ss}$  is given by

$$m = \text{int} \left[ \ln \left( \frac{\epsilon}{\phi - \phi_{ss}} \right) / \ln(L) \right] + 1 \dots\dots\dots (20)$$

where  $\text{int} [\cdot]$  is the integer function.

It can be shown that the time required to reach the fixed-point steady state  $\phi_{ss}$  is given by

$$T_c = mT_o W + \frac{(\phi(m) - \theta_o)}{\omega} \approx mT_o W \dots\dots\dots (21)$$

where  $\frac{(\phi(m) - \theta_o)}{\omega} \ll mT_o W$ .

Consequently, (21) shows the effects of both the amplitude and frequency of the input signal on the acquisition time. From (14), (16) and (21) it is evident that the lock range, input power sensitivity and the acquisition time can be controlled as desired using the adaptive controller block. The above equations are used

in the design of the controller block so as to optimize the performance of the CPD-DPLL for a given set of requirements as shall be demonstrated in the results section.

### 3. Noise Analysis

For the purpose of noise analysis, it is assumed that the incoming input signal is corrupted by an additive white Gaussian noise (AWGN) with zero mean and two-sided power spectrum density (PSD) of  $G_{nw}(f) = n_o/2$ , where  $n_o$  represents the noise power which is the same at all frequencies. Therefore, the autocorrelation can be given by the inverse Fourier Transform of  $G_{nw}(f)$  as  $R(\tau) = n_o \delta(\tau)/2$  where  $\delta(\tau)$  represents the Dirac Delta function <sup>(1),(18),(19)</sup>. As a result,  $R(\tau) = 0$  for  $\tau \neq 0$  so any two different samples of this kind of noise are uncorrelated and for this reason they are statistically independent <sup>(19),(20)</sup>.

Due to the discrete nature of the CPD-DPLL, statistical analysis of the phase error process can be obtained by studying the Chapman-Kolmogorov equation <sup>(7)</sup>. The noise samples  $\eta(k)$ 's are mutually independent for different values of  $k$ . Therefore, the phase error process  $\phi(k)$  can be regarded as a first-order, discrete time, and continuously variable Markov process which is also governed by modulo  $2\pi$ . The variable Markov process states that the first-order Markov process depends only on the previous state. As a result with a given initial phase error  $\phi(0)$ , the probability density function (pdf) of  $\phi(k)$  will satisfy the Chapman-Kolmogorov equation.

In the presence of noise, can be rewritten as

$$\phi(k+1) = \phi(k) - K'_1 \left[ \tan^{-1} \left( \frac{A \sin[\phi(k)]}{X} \right) \right] + K'_1 \eta(k) + \Lambda_o \dots\dots\dots (22)$$

where  $K'_1 = \omega G_1$  which results in  $K'_1 = K_1/W$  and  $W = \omega_o/\omega$ .

Since  $\phi(k)$  is independent of  $k$  and is a continuously variable Markov process, the transient response of the probability density function  $q_k(\phi|u)$  can be describe as

$$q_k(\phi|u) = \frac{1}{\sigma \sqrt{2\pi}} \exp \left[ - \frac{\left( \phi - u - K'_1 \left[ \tan^{-1} \left( \frac{A \sin[\phi(k)]}{X} \right) \right] + \Lambda_o \right)^2}{2\sigma^2} \right] \dots\dots\dots (23)$$

where  $\phi = \phi(k+1)$ ,  $u = \phi(k)$  and variance  $\sigma^2 = (K'_1)^2 \sigma_n^2$  with expectation mean as

$$E(\phi(k+1)|u) = u - K'_1 \left[ \tan^{-1} \left( \frac{A \sin[u]}{X} \right) \right] + \Lambda_o \dots\dots\dots (24)$$

which is independent of  $k$  due to the use of modulo  $2\pi$  process.

To find the mean, expectation of both sides of (22) is taken which yields

$$E(\phi(k+1)) = E(\phi(k)) - K'_1 E \left[ \tan^{-1} \left( \frac{A \sin[\phi(k)]}{X} \right) \right] + \Lambda_o \dots\dots\dots (25)$$

As the value of  $k$  approaches infinity, the stationary mean becomes

$$E \left[ \tan^{-1} \left( \frac{A \sin[\phi]}{X} \right) \right] = \Lambda_o / K'_1 \dots\dots\dots (26)$$

To linearize and simplify the equation for analysis purposes, the control signal is selected so that  $X = A$ . Therefore, (25) can be further simplified as

$$E \left[ \tan^{-1} \left( \frac{A \sin[\phi]}{X} \right) \right] \approx \sin[\phi] \approx \frac{X}{A} \frac{\Lambda_o}{K_1} \approx \frac{\Lambda_o}{K_1} \dots (27)$$

To derive the variance of phase error  $\sigma_\phi^2$ , (22) is squared and then the expectation is computed as

$$E[\phi^2] = E[\phi^2] - K_1'^2 E[(\delta)^2] + K_n'^2 \sigma^2 + \Lambda_o'^2 - E[\delta](2K_1' + 2K_1'\Lambda_o) + 2\Lambda_o E[\phi] \dots (28)$$

where  $\delta = \tan^{-1} \left( \frac{A \sin(\phi)}{X} \right)$

when the first-order CPD-DPLL is in the tracking mode and assuming that  $X = A$  then  $\tan^{-1} \left( \frac{A \sin(\phi)}{X} \right) \approx \phi$  for small  $\phi$  (rad) which results in

$$\sigma_\phi^2 = E[\phi^2] - \phi^2 = \frac{K_n'^2 \sigma_n^2}{K_1' \cos(\phi) (2 - \cos(\phi))} \dots (29)$$

where  $\phi_1$  (rad) is the locked state phase error. This is a linearized variance of the phase error with a mean of  $\phi_1$ , which results in a phase error pdf of

$$P(\phi) = \frac{1}{\sigma_n \sqrt{2\pi}} \exp \left( -\frac{(\phi - \phi_1)^2}{2\sigma_n^2} \right) \dots (30)$$

The theoretical probability density function (pdf) for different values of signal-to-noise ratio (SNR) is illustrated in Fig. 4. The pdf type of assessment is used to provide an indication of the noise effect on the phase error as discussed in the literature <sup>(1),(2),(16)</sup> so that the bell shape graph of the pdf becomes wider as the noise effect increases and vice versa. This figure shows the effect of the AWGN on the steady state phase error of the CPD. It is clearly shown that as SNR increases the steady state pdf increases. This will be demonstrated again through the simulation results in the next section.

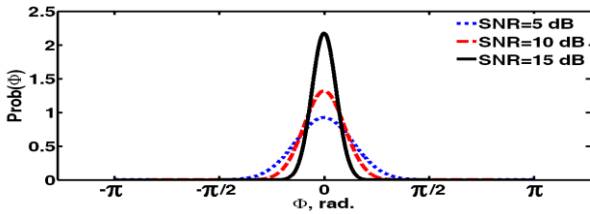


Fig. 4: Steady state phase error PDF of the first-order CPD-DPLL for different SNR values,  $K_1 = 1$ ,  $X=1$  and without frequency step.

#### 4. CPD-DPLL simulation results

The dynamic performance parameters of the CPD-DPLL system in terms of the lock range, acquisition speed, and noise is discussed in the following subsections. These parameters depend on customizing the adaptive controller to achieve the performance required by the particular application. The system performance features will be compared with those achieved by the conventional ZC-DPLL. A possible realization of the adaptive controller can be achieved using a frequency estimator, envelope detector and a Finite-State Machine (FSM). This provides the required adaptive controller output  $X$  values, which depend on the input signal

amplitude ( $A$ ) and frequency for the desirable performance.

**4.1 Lock Range** The lock range ( $M$ ) is defined here as the maximum tolerable deviation of the input signal frequency ( $\omega$ ) from the DCO free running frequency  $\omega_o$  at  $K_1 = 1$ . Fig. 5 illustrates the lock range as function of both adaptive controller output  $X$  and input signal amplitude  $A$  as will be investigated below.

As shown in Fig.3 (a) and (b), variations in the adaptive controller output  $X$  values are influenced by changes in  $A$ . This has different effects on the system lock range  $M$ . The relation between the lock ranges  $M$  and  $A$  for different controller output  $X$  values is shown in Fig. 5. Therefore, to compensate for variation in the input signal power, different adaptive controller output  $X$  values should be generated according to Fig. 5 to provide the required lock range. This implies that the lock range has to be fixed for a given range of signal amplitude  $A$ . For example, to set the lock range to 0.15, the adaptive controller should provide a value of  $X=2$  V for the input signal range of  $0 \text{ V} \leq A \leq 3 \text{ V}$  which eliminates the problem associated with the conventional ZC-DPLL. It is to be noted that the values for  $M$  in Fig. 5 represent the spread in the lock range around the frequency ratio  $W=1$  and loop gain  $K_1=1$  V.

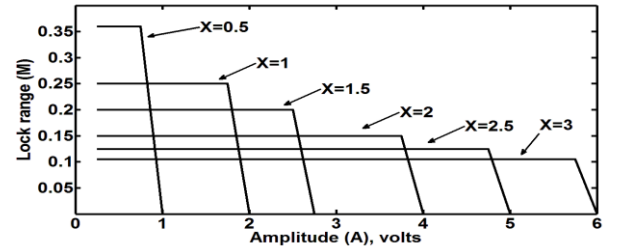


Fig. 5. Simulation results showing the variations in the lock range size ( $M$ ) with  $A$  and  $X$ .

**4.2 Acquisition** The acquisition time is the time required for the error signal  $e(k)$  to reach a steady state condition following a sudden change in the frequency of the input signal. This test can be performed by applying a step function to a voltage controlled oscillator that have the same free running frequency of the loop DCO as shown clearly in Fig. 2(a). Fig. 6 shows the response of the first-order CPD-DPLL to a positive input frequency step, of 20% above the starting frequency, of  $S=0.2$  V in comparison with the conventional ZC-DPLL. This test was accomplished for a loop gain of  $K_1 = 1$ , an input signal amplitude of  $A=2$  V, and a controlling output of  $X=2$  V. It can be seen from the transient response in Fig. 6 (b) that the CPD-DPLL system acquired lock within one clock cycle compared with eight clock cycles for the conventional ZC-DPLL. Similar results were obtained when negative steps were applied.

The system acquisition time performance under different frequency steps with various values of  $A$  and  $X$  was investigated as shown in Fig. 7. The plots indicate that there is a minimum acquisition time for particular values of  $A$  and  $X$  for different frequency steps. In particular, Fig. 7 (c) shows the acquisition time for particular values of the adaptive controller output  $X$  and with fixed value of  $A=1$  V for different frequency steps. Therefore, the adaptive controller needs to re-map the changes in both the amplitude and frequency of the input signal with the appropriate values to achieve the required acquisition time.

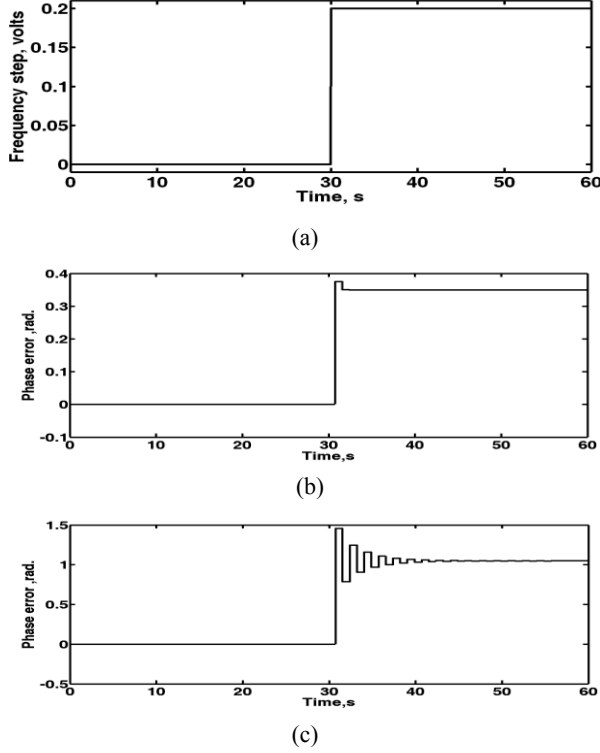


Fig. 6. (a) Positive step, (b) first-order CPD-DPLL transient response, and (c) first-order conventional ZC-DPLL transient response.

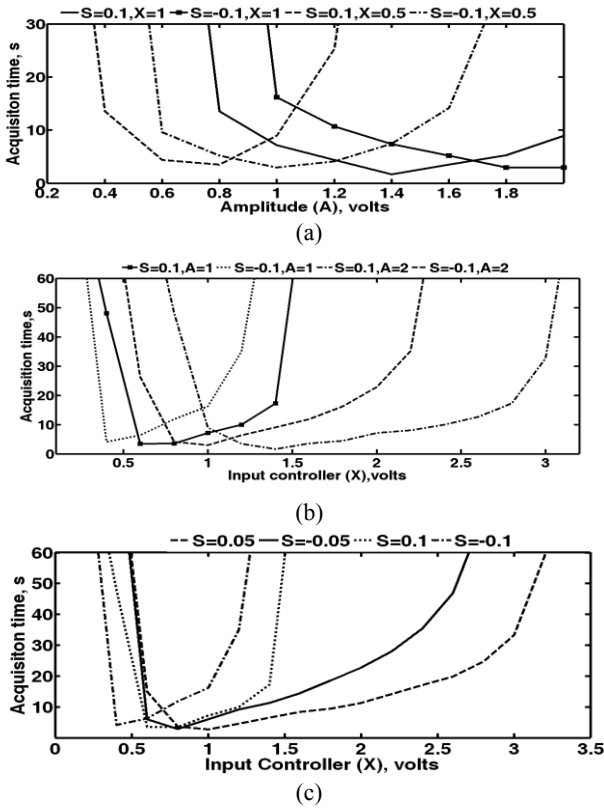


Fig. 7. Acquisition time as a function of X and A for different frequency steps (S).

The adaptive controller block that monitors changes in the input signal amplitude and frequency provides information so as to

generate the values of X required for a given performance goal. For example, Fig. 8 shows the effect of variations in A on the value of X for various frequency steps to achieve locking within one clock cycles. The plots in the figure are generated from Fig. 7 for minimum acquisition time. For example, assuming that  $A=1$  V,  $X=1$  V,  $K_1 = 1$ , and a frequency step  $S=-0.1$  V is applied, then the response of the CPD-DPLL is shown in Fig. 9 (a) which takes five clock cycles to reach the steady state. However, when the same conditions are applied to the adaptive controller algorithm of the CPD-DPLL a new value of  $X=0.6$  V is generated automatically to give a faster acquisition response as shown in Fig. 9 (b) within two clock cycles. These figures clearly show the improvement in the acquisition speed that can be achieved by the adaptive CPD-DPLL.

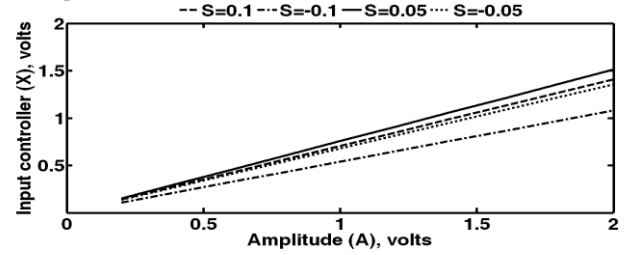


Fig. 8. Fast acquisition as a function of A, X, and frequency steps (S).

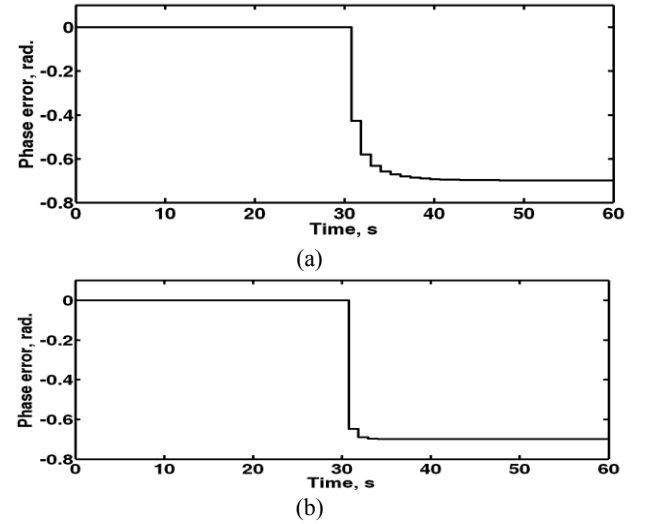


Fig. 9. (a) Adaptive CPD-DPLL response with  $X=1$  V, (b) adaptive CPD-DPLL response with  $X=0.6$  V.

**4.3 Noise performance** this section presents the effect of AWGN on the performance of the first-order CPD-DPLL. Some of the simulation results achieved are shown in Fig. 10 which illustrates the variation in the distribution for the phase changes, as the distribution becomes wider the noise has higher impact on the loop and vice versa. It can be seen from the plots that the system noise performance improves as the lock range decreases due to an increase in the adaptive controller output X value. However, as X decreases the lock range increases causing the noise performance of the system to degrade. It should be pointed out that decreasing the lock range leads to an increase in the system acquisition time and vice versa. Fig. 10 shows that the conventional ZC-DPLL has similar performance compared with the CPD-DPLL when  $X=0.94$  V is chosen. However, better



performance can be achieved with a selection of  $X=3$  V for different input signal SNR.

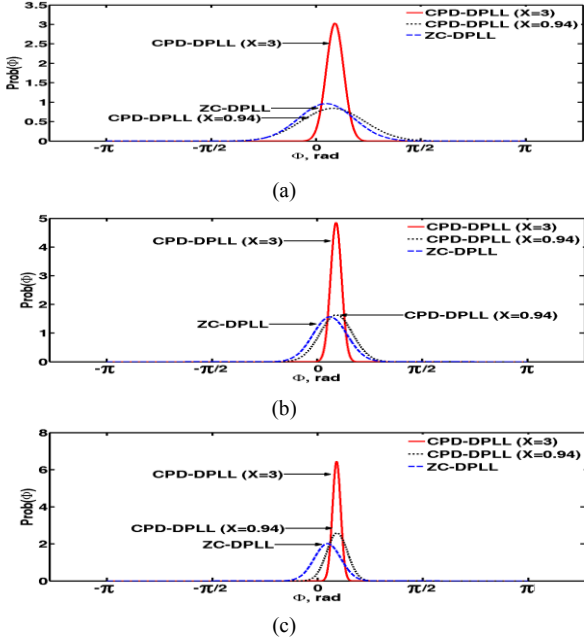


Fig. 10. Noise performance of CPD-DPLL and ZC-DPLL for (a) SNR=5dB, (b) SNR=10dB, and (c) SNR=15dB.  $A=1$  V,  $K_1 = 1$ , and frequency step  $S=0.05$  V.

The preceding sections of this paper established that the value of  $X$ , which is controlled by the adaptive controller, has direct impact on the system lock range, acquisition speed, and noise performance. This interdependency enables optimization of the CPD-DPLL to meet particular application requirements. For example, for some communication applications, such as global positioning systems <sup>(2),(21)–(23)</sup>, fast acquisition is required with a wider lock range in the transient state whereas in a steady state a narrow lock range is preferable so as to have better jitter and noise performances.

For example, in Fig. 11(d), for  $A=1$  V,  $K_1 = 1$ ,  $X=0.94$  V, and when the system is subjected to a frequency step of 0.05 V the transient response in Fig. 11 (b) shows that the system acquires lock within one clock cycle. Since the lock range is wide, fast acquisition achieved is at the expense of noise performance. However, under the same condition with a value of  $X=3$  V, i.e. narrower lock range, the system takes longer time to achieve lock as illustrated in Fig. 11 (c) but with much better noise performance. Hence, it is possible to design a system that has fast acquisition and improved noise performance by adaptively changing the value of adaptive controller output  $X$ . For all the above dynamic changes of the CPD-DPLL system the ZC-DPLL shows a fixed acquisition time similar to CPD-DPLL condition with a value of  $X=0.94$  V and lock range as depicted in both Fig. 11 (d) and Fig. 3 (c) respectively.

The impact of noise on the jitter performance of the CPD-DPLL compared with the conventional ZC-DPLL was evaluated and the results are shown in Fig. 12. It can be seen from the figure that the average jitter for the loop with wide lock range ( $X=0.94$  V) is higher than that with narrow range ( $X=3$  V). In addition, the figure shows that the jitter for ( $X=0.94$  V) is around three times higher when  $X=3$  V is used. Moreover, the figure

shows that the conventional ZC-DPLL has similar performance of the CPD-DPLL condition with a value of  $X=0.94$  V.

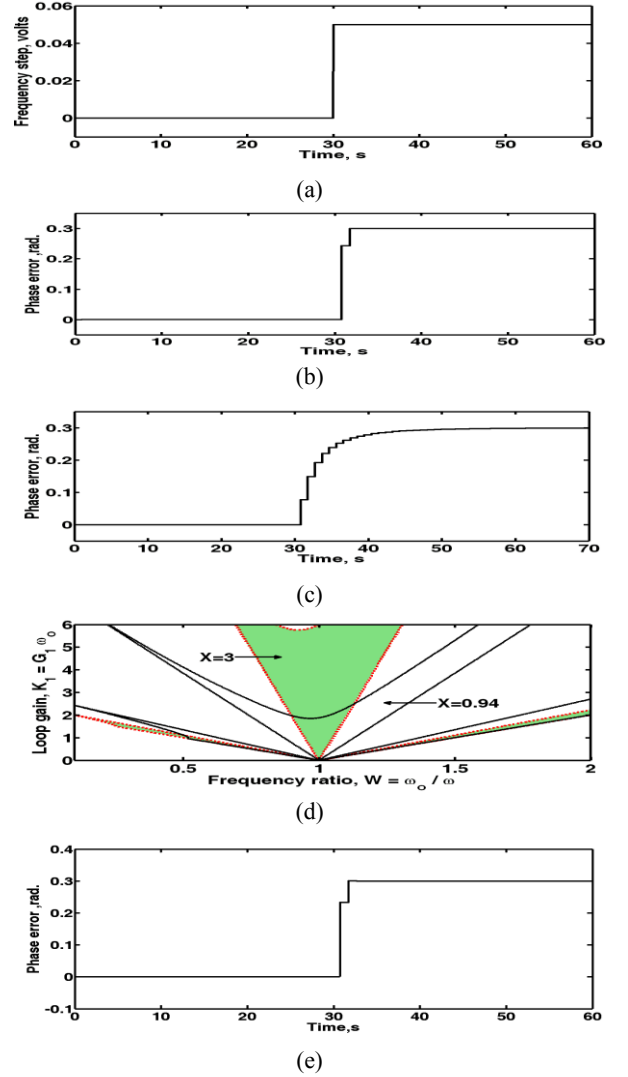


Fig. 11. (a) Positive input step, (b) transient response of the CPD-DPLL with  $X=0.94$  V, (c) transient response of the CPD-DPLL with  $X=3$  V, (d) lock range, and (e) transient response of the ZC-DPLL.

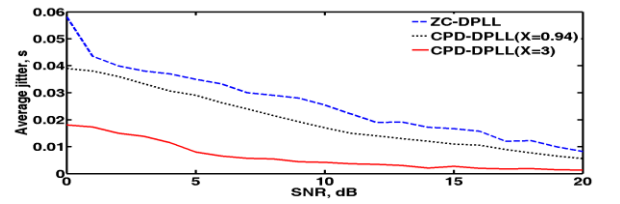


Fig. 12. CPD-DPLL and ZC-DPLL jitter performance for a range of SNR,  $A=1$  V,  $S=0.05$  V, and  $K_1 = 1$ .

## 5. CPD-DPLL FPGA implementation

In order to evaluate the performance of CPD-DPLL in real time, it was synthesized for FPGA implementation. The FPGA was preferred as the target technology due to the flexibility for reconfiguring and the ability to provide a fast prototyping system [24–26]. The Xtreme DSP development system from Xilinx /MATLAB-Simulink was used for the synthesis process <sup>(27),(28)</sup>. To compile the proposed CPD-DPLL design into a hardware description language (HDL) script, an initialization of the FPGA

A possible realization of the adaptive controller can be obtained by using an envelope detector and a FSM. Therefore, by customizing the requirements to cope with changes in the input signal amplitude, the adaptive controller will provide a constant value to suit the requirement. If the incoming signal changes from 0.8 V to 2 V, the lock range with an acceptable acquisition time, as shown in Fig. 13, will remain fixed by simply inserting a constant value of unity into the CPD phase detector to represent the output X of the adaptive controller as shown in Fig. 14. Fig. 13 also shows that the CPD-DPLL loop will not be affected by variations in the amplitude of the input signal down to zero but the acquisition will start to degrade below 0.8V.

Fig. 13. Variations of the acquisition time and lock range with input signal amplitude A for a fixed controller output X=1 V.

Fig. 14. FPGA Hardware implementation of the CPD-DPLL.

Additional gates are primarily needed for the CPD phase detector. It should be noted that the FPGA implementation of both the ZC-DPLL and the CPD-DPLL is only in a prototype form. Limited optimization, of the FPGA gate count, was applied because the implementation primary objective was to demonstrate the concept and the functionality of the proposed CDP-DPLL architecture in real-time application.

Fig. 15. Transient response of CPD-DPLL for FSK from 330 kHz to 400 kHz.

A non-uniform DPLL that uses a composite phase detector and an adaptive controller is proposed. The two main limitations exhibited by the conventional ZC-DPLL; the loop's nonlinearity and its sensitivity to input signal power have been overcome in the proposed CPD-DPLL loop. The CPD offers better linearity and hence improved lock range compared to the ZC-DPLL.

The inclusion of the adaptive controller block within the CPD-DPLL architecture gives the designer the flexibility to customize and optimize the overall system parameters, such as acquisition speed, lock range, and jitter, to best fit the particular application requirements. Depending on the form of implementation, be it FPGA or ASIC (application-specific integrated circuit), this flexibility can be exploited so that customization can be achieved through reprogrammable or reconfigurable implementations.



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